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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,431	07/31/2003	Hong Wang	42P15449	2852

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EXAMINER	
MOLL, JESSE R	
ART UNIT	PAPER NUMBER
2181	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/632,431	WANG ET AL.	
	Examiner	Art Unit	
	JESSE R. MOLL	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 October 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17-29,32 and 34-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11,12,15,18-21,23,25-28,32 and 34-37* is/are rejected.

7)☒ Claim(s) *10,13,14,17,22,24 and 29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 15 October 2009 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 4 and 5 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The use of "the control logic" qualified with the functionality of the logic to describe multiple logics is extremely confusing. Additionally, both claims lack antecedent basis for the second instance of control logic. Examiner suggests changing each instance of control logic to "a first control logic", "a second control logic", etc... This problem is compounded in claims such as claim 6 where “the control logic” is used alone to reference control logic.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-9, 11, 12, 18-21, 23, 25-28, 32 and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Purser et al. (A Study of Slipstream Processors) herein referred to as Purser, in view Solihin et al. (Prefetching in an Intelligent Memory Architecture Using a Helper Thread) herein referred to as Solihin.

6. Referring to claim 1, Purser discloses an apparatus comprising: a first processor (R-Stream Processor; see Figure 3) to execute a main thread instruction stream (R-Stream) that includes a delinquent instruction (any load which misses in the R-stream), wherein the first processor is to be associated with a first private cache (D-Cache and I-Cache of the R-Stream Processor); a second processor (A-Stream Processor; see Figure 3) to execute a helper thread instruction stream (A-Stream) that includes a subset of the main thread instruction stream (see first paragraph of page 7), wherein the subset includes the delinquent instruction (Any program will inherently include cache misses), wherein the second processor is to be associated with a second private data cache (D-Cache and I-Cache of the A-Stream Processor); a shared memory system (see page 4 regarding the A stream fetching data for the R stream) coupled to said first processor and to said second processor; and logic to retrieve, responsive to a miss of

requested data (any data not in L1 cache) for the delinquent instruction (instruction referencing data not in cache) in the private cache of the second processor (see section 2.3), the requested data from the shared memory system (when a load misses, the data must be fetched from the shared memory); the logic further to provide requested data to the first processor (through the Delay Buffer; see Figure 3).

Purser does not expressly disclose control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache associated with the second processor, the requested data to the first private cache associated with the first processor.

Solihin teaches control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache associated with the second processor, the requested data to the first private cache associated with the first processor (see the last 2 paragraphs of section 2.1 regarding push prefetching).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Purser by pushing data into the private cache of the first processor responsive to a miss as taught by Solihin in order to "effectively reduce the miss rates of the private caches, thereby improving the timeliness of prefetches." (see Solihin, third paragraph of section 2.1).

Regarding claim 3, Purser also discloses retrieval logic coupled to the control logic to retrieve the requested data from the shared memory system in response to the miss of the requested data for the delinquent instruction in the second private cache (Inherently,

if the data misses in the L1 cache, it must be requested from the L2 [or higher level memory]).

7. Regarding claim 4, Purser does not expressly discloses the control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to broadcast the requested data to an affinity group of processors including at least the first processor.

Solihin teaches control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to broadcast the requested data to an affinity group of processors including at least the first processor (see the last 2 paragraphs of section 2.1 regarding push prefetching; *note that the affinity group is a group containing only the first processor*).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have combined the inventions of Purser and Solihin as shown above regarding claim 1.

8. Regarding claim 5, Purser does not expressly discloses the control logic to push, responsive to a miss of requested data for the delinquent instruction in the second

private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to unicast the requested data to the first processor.

Solihin teaches control logic to push, responsive to a miss of requested data for the delinquent instruction in the second private cache, the requested data to the first private data cache of the first processor comprises the control logic, responsive to the miss of the requested data and the retrieval logic retrieving the requested data, to unicast the requested data to the first processor (see the last 2 paragraphs of section 2.1 regarding push prefetching).

It would have been obvious for one of ordinary skill in the art at the time of the invention to have combined the inventions of Purser and Solihin as shown above regarding claim 1.

9. Claim 6 recites limitations equivalent to those discussed above regarding claim 1.

10. Claim 7 recites equivalent limitations as claim 1 with the following exceptions which are taught by Purser. The claim is rejected for the same reasons stated above.

Purser discloses the second thread including a load instruction from the first thread that a miss to the first private cache is anticipated (see section 1 regarding the reasons for slipstreaming)

11. Claims 8 and 9 recite equivalent limitations as claims 4 and 5 and are rejected for the same reason.

12. Claim 11 recites equivalent limitations as set forth in claim in claim 1 and is therefore rejected using the same grounds as claim 1.

13. Regarding claim 12, Purser also discloses a third processor (see last paragraph of left column of page 2 regarding multiple cores) and a shared memory system coupled to said first processor and to said second processor (see page 4 regarding the A stream fetching data for the R stream), and said third processor.

14. Claims 18 and 25 recite equivalent limitations as claims 1 and is rejected for the same reasons.

15. Claim 19 recites limitations already discussed above regarding claim 4 and is rejected for the same reasons.

16. Claim 20 recites limitations already discussed above regarding claims 1 and 6 and is rejected for the same reasons.

17. Claim 21 recites limitations already discussed above regarding claims 1 and 4 and is rejected for the same reasons.

18. Claim 23 recites limitations already discussed above regarding claim 4 and is rejected for the same reasons.

19. Claim 25 recites limitations already discussed above regarding claim 1 and is rejected for the same reasons.

20. Claim 26 recites limitations already discussed above regarding claim 4 and is rejected for the same reasons.

21. Claim 27 recites limitations already discussed above regarding claim 1 and is rejected for the same reasons.

22. Claim 28 recites limitations already discussed above regarding claim 3 and is rejected for the same reasons.

23. Claims 32-37 recites limitations already discussed above and are rejected for the same reasons.

24. Claims 2 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Purser in view Solihin and Collins et al. (Speculative Precomputation: Long-range Prefetching of Delinquent Loads) herein referred to as Collins.

25. Regarding claim 2, Purser also discloses the first processor, second processor and logic are included within a chip package (see section 1.1 regarding CMP),

26. Purser does not explicitly disclose the shared memory system includes a shared cache.

27. Collins teaches the shared memory system includes a shared cache (see the third paragraph of page 16).

28. At the time of the invention, it would have been obvious for one of ordinary skill in the art to have modified the system of Purser to include a shared cache, as taught by Collins, in order to increase performance by using a fast shared memory.

29. Claim 15 recites equivalent limitations as claim 2 and is rejected under the same grounds.

Allowable Subject Matter

30. Claims 10, 13, 14, 17, 22, 24 and 29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Alford Kindred can be reached on (571)272-4037. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alford W. Kindred/
Supervisory Patent Examiner, Art Unit 2181

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